AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A computing apparatus comprising:

a digital data storage device;

a bus-to-bus bridge configured to receive digital data from a host processor and to forward said digital data to said digital data storage device in an encrypted form, wherein said bus-to-bus bridge is configured to encrypt said digital data and forward the digital data to the digital storage device without intervention of the host processor, and wherein a configuration register in the bus-to-bus bridge is adapted to store information that is used by the bus-to-bus bridge to selectively enable and disable encryption depending on the target device that is to receive the data that is transmitted via the bus-to-bus bridge;

a non-volatile memory location in or connected to said ~~logic circuit~~ bus-to-bus bridge which stores an identification code; and

a key accessed by said ~~logic circuit~~ bus-to-bus bridge to define at least in part an encryption process, wherein said key is derived at least in part from said identification code.

2. (Original) The computing apparatus of Claim 1, wherein said identification code is assigned to and associated specifically with said computing apparatus.

3. (Cancelled)

4. (Currently Amended) The computing apparatus of Claim 2 ~~3~~, wherein said ~~logic circuit~~ bus-to-bus-bridge is configured to verify said key without intervention by said host processor.

5. (Currently Amended) The computing apparatus of Claim 1, wherein said bus-to-bus bridge ~~logic circuit~~ additionally comprises a circuit for selectively disabling said logic circuit from encrypting said digital data.

6. (Original) The computing apparatus of Claim 1, wherein said key is derived in part from said identification code and in part from user input.

7. (Previously Presented) A computer comprising:

a plurality of data storage media drives;

a data path connected between said plurality of data storage media drives and a source of data for storage onto media associated with said data storage media drives; and

a bus-to-bus bridge coupled to said data path, said bus-to-bus bridge being configurable to enable encrypting of data being routed to a selectable subset of said plurality of data storage media drives, wherein said bus-to-bus bridge is configured to encrypt said digital data and forward said digital data to said data storage media drives without intervention of the host processor, and wherein a configuration register in the bus-to-bus bridge is adapted to store information that is used by the bus-to-bus bridge to selectively enable and disable encryption depending on the target device that is to receive the data that is transmitted via the bus-to-bus bridge.

8. (Original) The computer of Claim 7, wherein said plurality of data storage media drives includes one or more hard disk drives, and one or more floppy disk drives.

9. (Currently amended) The computer of Claim 7, wherein said bus-to-bus bridge ~~logic circuit~~ additionally comprises:

a non-volatile memory location which stores an identification code; and

a second memory location ~~coupled to said~~ ~~logic circuit~~ which stores an encryption key derived at least in part from said identification code, wherein said key is accessed by said bus-to-bus bridge ~~logic circuit~~ to encrypt said digital data for storage on said data storage media drives.

10. (Original) The computing apparatus of Claim 9, wherein said identification code is assigned to and associated specifically with said computer.

11. (Previously Presented) A data processing system comprising:

a data source;

at least one data storage device;

a logic circuit coupled to receive digital data from said data source and to route digital data to said data storage device, wherein said logic circuit is configured to encrypt said digital data and forward the digital data to the data storage device without intervention of a host processor, wherein the logic circuit comprises a bus-to-bus bridge;

a non-volatile memory coupled to said logic circuit with a serial data bus, said read only memory containing a hardware identifier;

a key register coupled to said logic circuit, said key register storing a key for performing data encryption, wherein said key is derived at least in part from said identification code; and

a configuration register coupled to said logic circuit, wherein said configuration register contains information enabling said logic circuit to perform encryption on digital data received from said data source using said key prior to storing encrypted digital data on said at least one data storage device, and wherein the configuration register is adapted to store information that is used by the logic circuit to selectively enable and disable encryption depending on the target device that is to receive the data that is transmitted via the bus-to-bus bridge.

12. (Original) The data processing device of Claim 11, further comprising at least two data storage devices, wherein said configuration register contains information enabling data encryption of data routed to a first one of said at least two data storage devices, and wherein said configuration register contains information disabling data encryption of data routed to a second one of said at least two data storage devices.

13. (Previously Presented) A circuit for encrypting data in a computing system comprising:

a first memory location storing an identification code; and

a logic circuit comprising a second memory location and an encryption engine, said logic circuit configured to receive said identification code from said first memory location and to store a key for use by said encryption engine, said key being derived at least in part from said identification code in said second memory location, wherein said logic circuit is configured to encrypt digital data and forward said digital data to a digital storage device without intervention of a processor, wherein the logic circuit comprises a bus-to-bus bridge, and wherein a configuration register in the bus-to-bus bridge is adapted to store information that is used by the logic circuit to selectively enable and disable encryption depending on the target device that is to receive the data that is transmitted via the bus-to-bus bridge.

14. (Original) The circuit of Claim 13, wherein said first memory location resides on a first integrated circuit, and wherein said logic circuit resides on a second integrated circuit separate from said first integrated circuit.

15. (Original) The circuit of Claim 14, wherein said first and second integrated circuits are coupled by a serial data bus.

16. (Previously Presented) A computer system comprising:

host computing logic, wherein said logic circuit is configured to encrypt digital data and forward said digital data to a digital storage device without intervention of a host processor, wherein the host computing logic is a bus-to-bus bridge, and wherein a configuration register in the bus-to-bus bridge is adapted to store information that is used by the logic circuit to selectively enable and disable encryption depending on the target device that is to receive the data that is transmitted via the bus-to-bus bridge;

means for storing an identification code associated with said host computing logic; and

means for deriving a key for data encryption at least in part from said identification code.

17. (Original) The computer system of Claim 16, wherein said means for deriving a key additionally comprises means for deriving a key at least in part from user input to said computer system.

18-21. Cancelled.